REMARKS

Claims 1-14, 16-20, 23-25 are pending. Claims 15, 21, and 22 were cancelled in a previous reply to a previous office action. Claims 1, 8, 20, and 23 are amended herein. No new matter has been added.

102(e) Rejections

Claims 1-14, 16-20, and 23-25

In paragraph 2 of the Office Action, Claims 1-14, 16-20 and 23-25 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. patent publication 2004/0019756 A1 (referred to hereinafter as "Perego"). The Applicant has reviewed the cited reference and respectfully submits that the present invention as recited in Claims 1-14, 16-20 and 23-25 is not anticipated nor rendered obvious by Perego.

Currently independent Claim 1 recites,

> A variable width memory system comprising:
> a bus for communicating information;
> a plurality of variable width memory locations coupled to said bus, said plurality of variable width memory locations store information, wherein said plurality of variable width memory locations receive a number of bits corresponding to the width of the variable memory locations; and
> a controller coupled to said bus, said controller directs access to said plurality of variable width memory locations, wherein said number of bits are potentially varied automatically on a per access basis depending on which variable width memory location of said plurality of variable width memory locations is being accessed.

With regard to independent Claim 1, Applicant respectfully states that Perego does not teach or suggest "wherein said number of bits are potentially varied automatically on a per access basis depending on which variable width memory location of said plurality of variable width memory locations is being accessed." For example, Perego teaches at paragraph 0004 that,

> Memory devices can be targeted to a wide variety of markets with very different sets of cost and performance constraints; consequently, the

optimal device width can vary significantly from one application to the next. Unfortunately, these variations make it difficult for memory suppliers and distributors to accurately predict the customer demand mix for memory devices of various widths... Furthermore, a memory device manufacturer may find that optimizing the cost for each target device width means a different design at the die level and potentially at the package level. This can increase the time-to-market and level of financial and engineering resources required to deliver each of these products to market.

Further at paragraph 0012, Perego states,

SDRAM 200 includes configuration logic 260 for setting the device width. Configuration logic 260 connects to mode register 220, and from there receives a memory width configuration value stored in register 220 during device configuration. Based on this information, configuration logic 260 configures a data control circuit 265, a latch circuit 270 and an input/output (I/O buffer 275 to obtain the device width associated with the memory-width configuration value.

Thus, Perego discloses a method for manufacturing a memory device that can be configured at the manufacturers to have different widths depending on the target device that the memory device will be shipped with. It is respectfully submitted that in Perego's invention the number of bits that are to be accessed for the memory device is configured once "during device configuration" at the manufacturers and therefore, remains constant after the memory device is shipped. To do differently, would defeat the purpose of Perego's invention. Further, all of the data stored on a particular Perego system would be stored using the same memory-width, whereas, data stored on a particular variable width memory system as recited in Claim 1 could be stored using different widths and hence the number of bits for accessing the locations storing the data could potentially vary on a per access basis automatically. Therefore, Perego does not teach or suggest "wherein said number of bits are potentially varied automatically on a per access basis depending on which variable width memory location of said plurality of variable width memory locations is being accessed," as recited in Claim 1.

The Office Action dated December 16, 2004 states at paragraph 3 of the "Response to Arguments" section:

> ...Perego discloses the configuration logic determines the number of memory banks to be selected and depending on this determination, the device width is selected. Therefore, the memory width can be changed if the configuration is changed (Page 4, paragraph 0047). The memory width depends on the memory bank configuration and **being that the memory has variable widths, the number of widths accessed depends of the current width of the memory location accessed.**

Note, paragraph 0046 of Perego does not state "...being that the memory has variable widths, the number of widths accessed depends of the current width of the memory location accessed."

> However, what Perego actually says at paragraph 0047 is the following: Configuration logic 310 determines which of physical banks PB0-PB3 are selected, and consequently which bank-selected signals are asserted, based upon the selected device width and memory address. The following Table summarizes the logic within configuration logic 310 that generates the appropriate bank-selected signals.

Applicant respectfully agrees with the Office Action's statement that "Perego discloses that configuration logic determines the number of memory banks to be selected and depending on this determination, the device width is selected." More specifically, as already stated herein, Perego discloses a method for manufacturing a memory device that can be configured at the manufacturers to have different widths depending on the target device that the memory device will be shipped with. It is respectfully submitted that in Perego's invention the number of bits that are to be accessed for the memory device is configured once "during device configuration" at the manufacturers and therefore, remains constant after the memory device is shipped. Since, the number of bits accessed is configured at the manufacturers it is not possible for Perego to teach or suggest "wherein said number of bits are potentially varied automatically on a per access basis depending on which variable width memory location of said plurality of variable width memory locations is being

accessed," as recited in Claim 1. It is respectfully submitted that Perego's system would have to be shipped back to the manufacturers for re-configuration between every access in order to vary the number of bits between accesses, which would render Perego's invention useless. Furthermore, shipping Perego's system back to the manufacturers would not be varying the number of bits... automatically, as Claim 1 recites. Therefore, Perego does not teach or suggest "wherein said number of bits are potentially varied automatically on a per access basis depending on which variable width memory location of said plurality of variable width memory locations is being accessed," as recited in Claim 1. Claims 2-7 depend on Claim 1 and recite additional limitations and therefore should be patentable for the same reason that Claim 1 should be patentable.

Applicant respectfully submits that currently independent Claim 8 should be patentable for similar reasons that Claim 1 should be patentable in that Claim 8 recites, "potentially varying the bit capacity of said register on a per accesses basis to memory cells automatically." Claims 9-14, 16-19 depend on Claim 8 and recite additional limitations and therefore should be patentable for the same reason that Claim 1 should be patentable.

Applicant respectfully submits that currently independent Claim 20 should be patentable for similar reasons that Claim 1 should be patentable in that Claim 20 recites, "wherein the number of said bits are potentially varied automatically on a per accesses basis to portions of said blocks of data when identifying said bits and said width varies on a per accesses basis when assigning a memory location that is equal to the number of said bits."

Applicant respectfully submits that currently independent Claim 23 should be patentable for similar reasons that Claim 1 should be patentable in

that Claim 23 recites, "wherein the number of bits returned by said means for storing information are potentially varied automatically per read request due to which of said uniquely identifiable different width memory locations is being accessed by said read request." Claims 24 and 25 depend on Claim 23 and recite additional limitations and therefore should be patentable for the same reason that Claim 1 should be patentable..

Conclusions

In light of the above remarks, Applicants respectfully request reconsideration of the rejected claims.

Based on the arguments presented above, Applicants respectfully assert that Claims 1-25 overcome the rejections of record and, therefore, Applicants respectfully solicit allowance of these claims.

Applicants have reviewed the references cited but not relied upon and respectfully submit that these references neither teach nor suggest the claimed limitations.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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